Fabrication of carbon nanotube-based nanodevices using a combination technique of focused ion beam and plasma-enhanced chemical vapor deposition

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This study focuses on the fabrication of two nanodevice prototypes which utilized vertical and horizontal carbon nanotubes used the focused ion beam to localize the catalysts, followed by plasma-enhanced chemical vapor deposition. First, metal-gated carbon nanotube field emitter arrays were fabricated on multilayer substrates containing an imbedded catalyst layer. Second, horizontally aligned single-walled carbon nanotubes were grown on a transmission electron microscopy grid. This allows the carbon nanotubes to be directly analyzed in a transmission electron microscope. It is expected that the methodology introduced here will open up opportunities for the direct fabrication of carbon nanotube based nanodevices. © *2007 American Institute of Physics*.
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In this study, we demonstrate an effective method of combining the focused ion beam (FIB) technique and the chemical vapor deposition process for synthesizing carbon nanotubes (CNTs), creating triode-type multiwalled carbon nanotube (MWCNT) array of field emitters, and fabricating single-walled carbon nanotube (SWCNT) based nanodevices.

Vertically aligned CNTs show a great potential for field emitter applications. The small radius of curvature of CNT tips makes them ideal for low-voltage field emission devices such as flat-panel displays.

Furthermore, CNTs show potential as microdevice interconnects.[1] As wire width decreases (<32 nm), traditional aluminum (Al) or copper (Cu) interconnects in high performance "very large scale" integration systems will suffer significant resistance increases due to grain boundary scattering.[2] Increased resistance will result in delay and electromigration problems, limiting performance and reliability.[3] Thus, in recent years, the search for new, miniaturized, and more effective on-chip interconnects has been the major focus in nanodevice research. Vertically aligned CNTs (those grown perpendicularly to the substrate) have been demonstrated as a promising replacement. They boast tiny widths, excellent conductivity, and superior current carrying capacity. For example, CNTs have been reported with current densities exceeding 10^9 A/cm^2, more than 1000 times greater than the maximum current density of silver or copper.[4,5]

Horizontally aligning CNTs between two electrodes with controlled properties is one of the significant challenges in field-effect transistor (FET) applications. The most common method for fabricating a CNT FET begins with a sonicated dispersion of existing CNTs, followed by the distribution of the CNTs onto a substrate with predefined electrodes.[6] Here, a method is developed to synthesize CNTs directly between metal electrodes. This method also allows for direct observation of as-made CNTs by transmission electron microscopy (TEM). The traditional method for preparing such TEM samples is time consuming and requires several stages of sample preparation (removal of the CNTs from the substrate, suspension of the CNTs in a solvent, and finally the placement of the CNTs onto a TEM grid). Through this type of sample preparation, it is not only randomly picking up CNTs for characterization but also introducing defects. The method introduced here, however, avoids any sample preparation procedures that may alter the structure of the CNTs.

During the fabrication of metal-gated carbon nanotube field emitter arrays (MG-CNT-FEAs), instead of depositing the catalyst into milled holes, a common practice in other reports,[7–9] a multilayer structure with an embedded catalyst layer was used. To construct this structure, an indium tin oxide (ITO) adhesion layer of 15 nm was deposited on a silicon substrate, and a 10 nm thin film of Ni, serving as the catalyst for CNT growth, was sputter coated over it. A 1 μm thick layer of insulating SiO_2 was deposited onto the Ni catalyst. Following this, another 15 nm ITO adhesion layer and a 120 nm thin film of Pt were deposited on top of the SiO_2 by magnetron sputtering. The Pt layer served as the gate electrode. A schematic diagram of the substrate design is shown in Fig. 1(a). A FEI dual-beam SEM/FIB was then used to

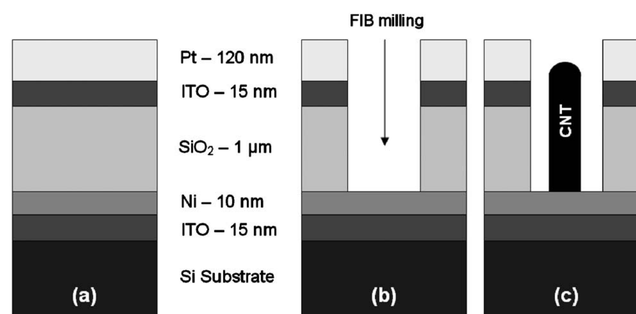

FIG. 1. (a) MG-CNT-FEA sample design including Pt gate, SiO_2 insulating layer, embedded Ni catalyst, and ITO adhesion layers. (b) and (c) Preparatory FIB milling and result of CNT synthesis.

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mill arrays of holes (300 nm–1 μm in diameter) to expose the Ni catalyst for the CNT growth, as illustrated in Fig. 1(b).

It was found that a method to fabricate MG-CNT-FEAs using the photolithography to etch arrays of holes into a silicon substrate followed by the sputter coating of Fe into the holes to supply a catalyst has been reported.[10] However, the catalyst island deposited by this procedure often yields undesired CNT growth regions which require an additional procedure for removal. In our method, we utilized the FIB to selectively expose the predeposited catalyst. This procedure has proved to be significantly easier than the deposition of a catalyst into preetched regions through sputtering, evaporation, or electrochemical deposition. In this process, control over the milled depth and geometry as it pertained to the exposed catalyst became the single crucial factor in substrate preparation. The challenge for determining the milling depth of a multilayer structure is that each layer of different materials has a different milling rate. It is therefore necessary to calibrate the settings (beam current and milling time) for a particular pattern to achieve the desired depth. Deviations in the depth of emitter holes can be reduced by milling for a greater period of time at a reduced beam current.

Once the gates had been fabricated and the catalyst exposed, vertically aligned CNTs were synthesized in each gated cavity using the plasma-enhanced chemical vapor deposition (PECVD) (Nanoinstruments Black Magic). During synthesis, the substrates were heated to 725 °C and exposed to 50 SCCM (SCCM denotes cubic centimeter per minute at STP) of C_2H_2 and 200 SCCM of NH_3 gas for approximately 30 min. This process transformed the Ni thin film into Ni nanoparticles which then served as the catalysts for CNT growth. C_2H_2 was introduced as a carbon source, while NH_3 etching prevented the formation of amorphous carbon. During the PECVD process, the silicon substrate was biased to a negative potential of 630 V which formed a glow discharge plasma. The CNTs grown by PECVD were vertically aligned due to the large electric field within the plasma sheath on the cathode. A FEI Sirion field emission SEM and a Tecnai F-20 field emission TEM/STEM equipped with an energy-dispersive x-ray spectrometer were used to characterize the morphologies and internal structures of the synthesized nanotubes.

SEM characterization revealed variation in CNT morphology (Fig. 2). The results displayed three distinct morphological variables: bundling, CNT diameter, and height which can be controlled by changing the milling and growth parameters. The first of these three, individual thick nanofibers [Figs. 2(I)(a)–2(I)(c)] was produced by milling a large diameter hole to the exact depth of the Ni layer. Accurate milling to the catalyst layer allows tip growth from the entire exposed Ni surface. A second category of thinner CNTs was synthesized without changing the diameter of the hole [Figs. 2(II)(a)–2(II)(c)]. Note that penetrating the catalyst layer, rather than just uncovering it, sputtered Ni particles onto the inner walls of the hole, resulting in bundles of thin CNTs. Previous study suggests that both types of nanotubes or nanofibers could serve as replacements for vertical interconnects in microchips.[11]

A third CNT morphology was synthesized by decreasing the diameter of the milled hole to ~300 nm, while maintaining the Ni-layer milling depth and the same growth conditions for the single CNTs. The only difference is the reduction of the diameter of the milling holes [Figs. 2(III)(a)–2(III)(c)]. Thin CNTs, grown individually, appear most promising as field emitters. Finally, the height of the CNT in relation to the gate layer can be controlled by limiting the plasma exposure time during PECVD growth. For the gate to effectively enhance field emission, nanotubes must remain below the gate layer. A reduced plasma time (and therefore overall growth time) of approximately 15 min will allow the CNTs to attain heights slightly below the gate layer. A CNT of ideal height for gated emitters is demonstrated in Fig. 2(III)(d). However, it is much easier to image, characterize, and determine the yield of taller CNTs.

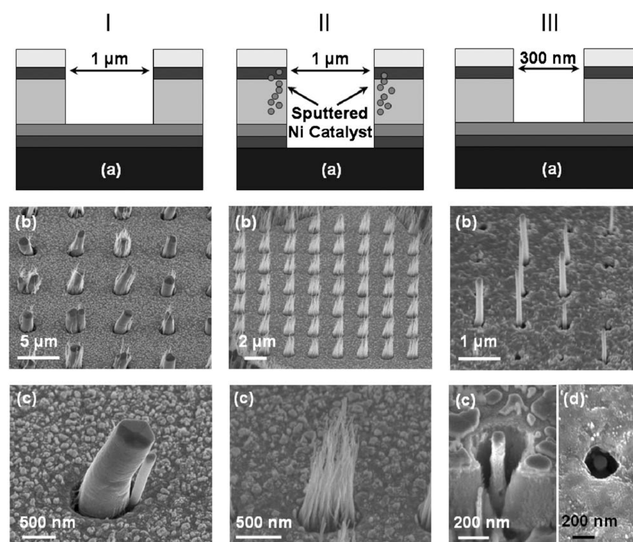

FIG. 2. (I) Nanofibers and CNTs fabricated within microgated cells by FIB milling for holes which are approximately 1 μm wide milled to the catalyst layer, (II) milled beyond the catalyst and ~1 μm in diameter, and (III) 300 nm wide and as deep as the Ni layer. (III) (d) Shorter CNTs produced by reduced plasma exposure during synthesis.

In this study the growth of horizontally aligned SWCNTs utilized a slightly different substrate to ease TEM characterization. A Si_3N_4 membrane window TEM grid was fabricated with a window thickness of 50 nm and a surrounding silicon support 200 μm thick. A thin film catalyst consisting of Al (15 nm)/Fe (1 nm)/Mo (0.3 nm) was deposited onto the Si_3N_4 membrane grid via a sputter coater (Ref. 6). The thickness of these catalyst layers was controlled with a quartz-oscillator thickness monitor. The FIB was then used to mill a series of trenches completely through the Si_3N_4 membranes [Fig. 3(a)]. This substrate was placed in a CVD chamber with a base vacuum of ~0.1 mbar. The temperature was ramped to 950 °C at a rate of 300 °C/min. Once the desired temperature was reached, acetylene was fed into the chamber at a flow rate of 200 SCCM as a carbon source. The nanoparticles produced from melting the thin film reacted with the gaseous C_2H_2, leading to the formation of SWCNTs.[12]

Suspended CNT networks with well-defined orientations within these trenches are visible in Figs. 3(b) and 3(c). As the gap width was increased, the nanotube density decreased. The maximum growth distance was approximately 2.5 μm. In this growth process, although the CNTs were well aligned horizontally from one side of the trench to the other, no external driving force such as plasma or an electric field was applied to the growth process. It is plausible that the growth direction of the CNTs was driven by van der Waals forces.[13] In high resolution TEM images [Figs. 3(d) and 3(e)], the wall

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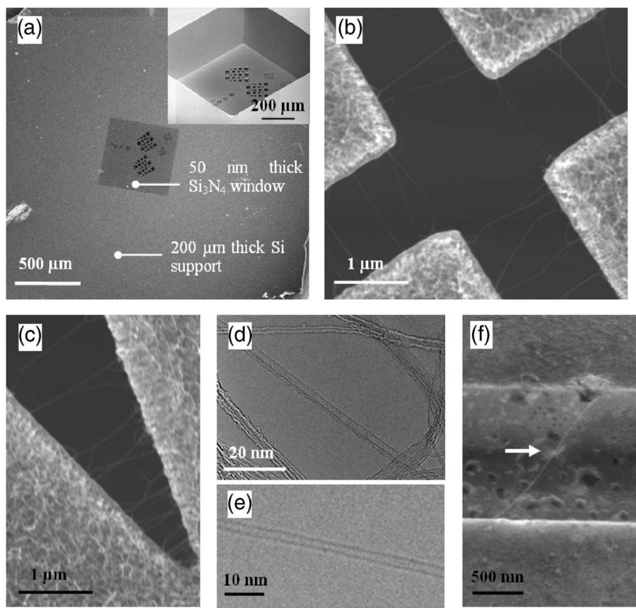

FIG. 3. (a) SEM image of Si_3N_4 membrane window with surrounding silicon support. The insert image shows the reverse side of this TEM grid. (b) and (c) Suspended networks with well-defined orientations grown within trenches shown in (a). (d) TEM images showing bundles of SWCNTs. (e) Isolated SWCNTs. (f) SEM image of SWCNTs grown across two electrodes in Si substrate.

structure of an individual SWCNT is clearly observed. These suspended bridges are individual or bundled SWCNTs with a diameter of approximately 1–3 nm. These results are consistent with those reported by Choi *et al.*,[14] whose work featured the fabrication of CNTs on a micromachined silicon grid using thermal oxidation, an ion-implanted catalyst, and wet etch and dry etch methods.

The method introduce here can be used to synthesize both MWCNTs and SWCNTs. To verify the morphology of the CNT samples of either MWCNTs or SWCNTs with high growth density, Raman spectroscopic analysis was performed using an excitation line at 488 nm. Figure 4 shows the Raman spectra of MWCNTs and SWCNTs grown at 750 and 950 °C, respectively. The SWCNT spectrum revealed a typical radial breathing mode (RBM) peak around 186 cm^{-1}, corresponding to the disordered carbon band (*D* band,

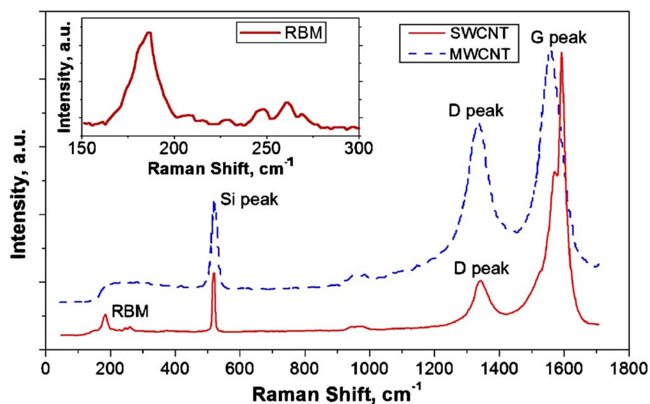

FIG. 4. (Color online) Raman spectrum of SWCNTs and MWCNTs on Si substrate. The inset shows a high resolution RBM peak around 186 cm^{-1}.

around 1344 cm^{-1}) and highly ordered graphite band (*G* band, around 1593 cm^{-1}). The $G:D$ peak ratio of SWCNTs (5.4) was larger than that of MWCNTs (1.3), which confirmed that the quality of SWCNTs was better than that of MWCNTs. The *G* peak high wave number shift (30 cm^{-1}) of SWCNTs with respect to MWCNTs further validated the high quality of the SWCNTs.

To explore the direct fabrication of a CNT FET, this method was then applied to synthesize SWCNTs across trenches milled into a Si wafer [Fig. 3(f)]. Electrodes can then be deposited at either end of the CNT to allow for testing the contact resistance. It also allows studying the effect of adsorbates and substrate temperature on the reduction of the contact resistance (currently in progress). It is expected that the direct growth of CNTs should be able to minimize the substrate-to-CNT contact resistance (typically on the order of kilohms or megaohms), a factor that frequently interferes with tests performed in the traditional dispersion and alignment methods.[15,16]

In summary, two types of prototyping nanodevices were explored by growing vertically and horizontally aligned CNTs on designed substrates. The fabrication of MG-CNT-FEAs was accomplished using a substrate containing an embedded catalyst and fabricated by a combination of FIB milling and PECVD synthesis of CNTs. Also presented was a technique to synthesize horizontally aligned SWCNTs to allow direct investigation of their properties as potential metal oxide semiconductor field effect transistors.

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